**3.5 Latch-Up**

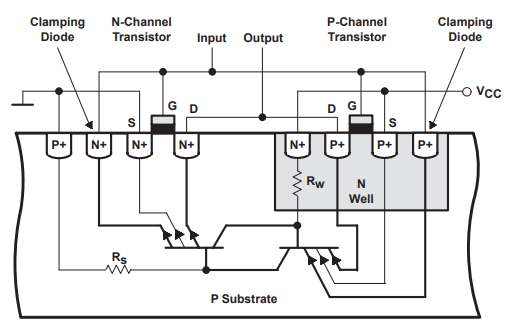
****Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path. CMOS and BiCMOS circuits use NMOS and PMOS transistors to create the circuit functions. In the design of the CMOS integrated circuit, the proximity of the PN junctions that form the NMOS and PMOS transistors create inherent parasitic transistors and diodes. These parasitic structures create PNPN Thyristors, also called silicon-controlled rectifiers (SCRs). Excursions (overshoots and undershoots) outside the normal operating voltage and current levels can trigger PNPN Thyristors and may cause Latch-Up. Latch-Up is not a risk if the voltage and current levels applied to the device adhere to the absolute maximum ratings. The parasitic thyristor structure that causes latch-up is formed due to the interactions between the PNP and NPN bipolar transistors that are present in the integrated circuit. When the voltage across the base-emitter junction of the PNP transistor exceeds a certain threshold, a parasitic NPN transistor is formed between the PNP collector and the NPN base. Similarly, when the voltage across the base-emitter junction of the NPN transistor exceeds a certain threshold, a parasitic PNP transistor is formed between the NPN collector and the PNP base. Once these parasitic transistors are formed, they can conduct current between the power supply rails, leading to latch-up , see figure 3.17. [1]

Figure 1. Parasitic Transistors in a CMOS Circuit

Latch-up is a significant problem in analog circuit layout design, as it can cause damage to the circuit and l ead to circuit failure. It is caused due to the interaction of parasitic transistors that are inherent in the layout of a standard CMOS transistor. When the circuit is powered up, the parasitic transistors interact with each other, creating a feedback loop that can cause the circuit to lock up in a conducting state. The excess current creates heat, which can cause damage or even destroy the circuit. Latch-up is an important consideration in analog circuit layout design, and careful attention to the layout and component placement can help avoid the problem and ensure a reliable and robust circuit. It's important to note that latch-up is not specific to analog circuits and can occur in digital circuits as well. However, the effects of latch-up in digital circuits are generally not as significant as in analog circuits. For example, in digital circuits, the latch-up may cause a delay in switching, but it is unlikely to cause damage to the circuit. [1]

**3.5.1 Latch Up types**

1. **Undershoot latch-up** refers to a type of latch-up that occurs when a voltage undershoot (a temporary decrease in voltage) triggers an internal parasitic bipolar transistor in a CMOS circuit. During undershoot latch-up, the substrate diode of the parasitic transistor becomes forward-biased and conducts, causing a large current to flow through the device. This can lead to the device getting stuck in a high-current and potentially destructive state until the power supply is turned off. Undershoot latch-up can happen in a variety of situations, such as when there is a sudden decrease in the power supply voltage, when the circuit is subjected to electromagnetic interference (EMI), or when there is a large current flowing through the circuit. The risk of undershoot latch-up can be mitigated through proper design techniques such as using guard rings and designing a well-balanced layout . [2]
2. **Overshoot latch-up** as a type of latch-up that can occur in certain situations. Overshoot latch-up can occur when a voltage overshoot (a temporary increase in voltage) triggers an internal parasitic bipolar transistor in a CMOS circuit. The overshoot may cause a high voltage to be applied to the gate of the parasitic transistor, causing it to become forward-biased and conductive. As a result, a large current can flow through the device, leading to latch-up. Overshoot latch-up is a less common type of latch-up compared to undershoot latch-up, but it can still occur in certain situations, for example when there is a sudden increase in the power supply voltage, or when the circuit is subjected to electromagnetic interference (EMI). Proper design techniques such as guard rings and a well-balanced layout can also help reduce the risk of overshoot latch-up . [2]

**3.5.2 Latch up Prevention**

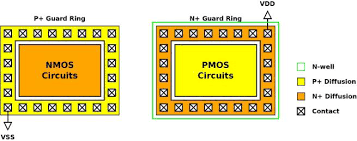
Latch-up is often caused by design flaws rather than manufacturing defects. It can be avoided by proper layout design, which involves placing critical components in specific locations and taking into account the parasitic effects of the components. Simulation tools can be used to predict and analyze the behavior of the circuit and identify potential latch-up conditions before the physical layout is created. Additionally, Spacing of the elements of each transistor, diode, resistor and capacitor are now being controlled through process characterization and design rules to help minimize the effect of current or voltage pulses on the products. Additionally, guard rings have been added around known radiators in the circuits or if spacing concerns are critical around individual PMOS and NMOS transistors, diodes or substrate resistors. Guard rings act as injected carrier syphons allowing these carriers to flow to the supply or ground. Also, the use of substrate ties and well taps act as excited carrier syphons and are guided by design rules for placement. These ties and taps are necessary for Latch-Up immunity. Another very effective method of quenching Latch-Up is to use an EPI (epitaxial silicon) layer. The EPI layer is doped appropriately for the best transistor performance (more lightly doped than the remaining lower portion of the substrate that is highly doped). The highly doped substrate directs majority carriers to ground and reflects minority carriers making the guard rings more effective (see Figure 2). Even with these safeguards, there is a possibility of parasitic transistors in circuits that are not identified. These unidentified Latch-Up sources need to be identified; one way is a Latch-Up stress test.

Figure 2. Guard Rings in a CMOS Circuit

In conclusion, avoiding latch-up is essential for the successful design and performance of analog circuits. Careful layout design, modeling, and simulation can help identify potential latch-up conditions and prevent them. Additionally, testing and validation ensure that the final design is robust, reliable, and meets the required specifications .

**3.5.3 Latch-Up Test**

Latch-up test circuits are used to test the susceptibility of integrated circuits (ICs) to latch-up, The latch-up test circuit is designed to simulate the conditions that can cause latch-up in an IC. It consists of a power supply, a voltage source, and a current source. The power supply provides the voltage and current necessary to activate the parasitic transistor. The voltage source is used to apply a voltage to the IC, while the current source is used to apply a current to the IC , see Figure( 3.5.3). The test circuit is connected to the IC under test and the power supply is turned on. The voltage source is then adjusted to the desired level and the current source is adjusted to the desired level. The voltage and current levels are then monitored to ensure that they remain within the specified limits. If the voltage or current levels exceed the specified limits, the test circuit is shut off and the IC is examined for any signs of latch-up.

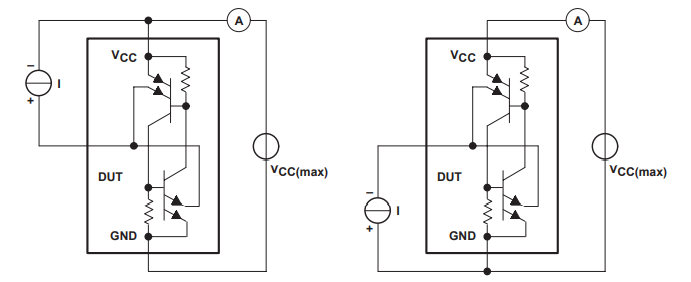


Figure (3.5.3). Latch-Up Test Circuit

The latch-up test circuit is an important tool for ensuring the reliability of ICs. It can help identify potential problems before they become serious, and can help prevent costly failures. It is also important to note that the test circuit should be used in conjunction with other tests, such as thermal testing, to ensure that the IC is functioning properly.

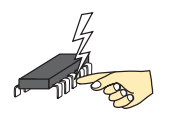
**3.6 Electrostatic discharge (ESD)**

Electrostatic discharge (ESD) is a phenomenon that occurs when two objects of different electrical potentials come into contact, resulting in a sudden flow of electricity between them . Walking across the floor, for example, causes the buildup of charge on the human body. Touching a conducting object can result in a transfer of charge or a static "shock." If the transfer of this charge (the discharge of the electrostatic charge buildup on the human body) is through the thin gate oxide (GOX) of a MOSFET, it is likely that the GOX will be damaged. While we use the human body as the location of the buildup of electrostatic charge, just about any object can build up charge. In analog circuits, ESD can cause damage to sensitive electronic components, and therefore, it is important to design circuits with ESD protection in mind.

**3.6.1 ESD Testing Models**

There are several simulation and testing techniques that can be used to validate the effectiveness of ESD protection measures in analog layout circuits. These techniques can help designers to optimize their ESD protection strategies, identify potential vulnerabilities, and ensure that the circuit meets the required standards for operation in harsh environments. [2]

1. **Human-Body Model**

One common testing technique for ESD protection is the Human Body Model (HBM), which simulates the effects of a human body coming into contact with a circuit. HBM testing involves applying a high-voltage pulse to a circuit, simulating the effect of a human touching the circuit while charged with static electricity.

The HBM ESD protection circuit is designed to withstand a discharge of 2 kilovolts (kV) to 8 kV with a rise time of about 1 nanosecond (ns). The HBM ESD protection circuit consists of three components: a series resistor, a diode, and a shunt capacitor. The series resistor limits the current flowing into the circuit during an ESD event, while the diode and shunt capacitor provide a discharge path for the ESD energy,for example the circuit in Figure 4.

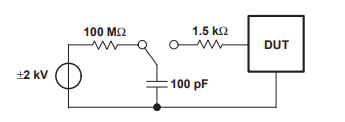
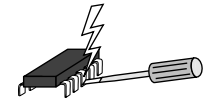


Figure 4. Human-Body Model Test Circuit

The HBM ESD protection circuit is placed between the input and output of the analog circuit. The series resistor should be placed as close as possible to the input of the circuit to limit the current flow. The diode should be placed as close as possible to the circuit input to provide a discharge path for the ESD energy. The shunt capacitor should be placed as close as possible to the output of the circuit to reduce the voltage across the circuit. [2]

It is important to note that the HBM ESD protection circuit may affect the performance of the analog circuit. The series resistor can introduce a voltage drop, and the diode and shunt capacitor can affect the signal frequency response. Therefore, careful consideration and optimization of the ESD protection circuit are required to minimize the impact on the circuit's performance. [2]

1. **Machine Model**

Another common testing technique is the Machine Model (MM), which simulates the effects of ESD events that occur during circuit manufacturing and testing. MM testing involves applying a high-voltage pulse to a circuit, simulating the effects of electrostatic discharge during handling and testing of the circuit.

The MM consists of lumped circuit elements such as resistors, capacitors, and diodes, which are used to model the ESD protection devices and the parasitic elements in the circuit ,for example the circuit in Figure 5.

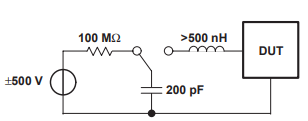
The MM is created by analyzing the layout and extracting the relevant parasitic elements and ESD protection devices. Once the MM is created, it can be used to simulate the performance of the circuit and optimize the layout for ESD robustness. [2]

Figure 5. Machine-Model Test Circuit

The MM can be used in conjunction with ESD simulation tools to predict the ESD performance of the circuit. The ESD simulation tools use the MM to simulate the ESD event and predict the voltage and current distribution in the circuit. The results of the simulation can be used to optimize the layout for ESD robustness by adjusting the placement and sizing of the ESD protection devices. [2]

1. **Charge Device Model**

Charge Device Model (CDM) is a type of Electrostatic Discharge (ESD) testing methodology used to evaluate the ability of a device to withstand electrostatic discharges. In CDM, a charged device is rapidly discharged through a low impedance path, simulating a sudden discharge that may occur during normal use or handling of the device. The discharge is initiated by touching the charged device with a conductive probe, which provides a low impedance path for the discharge current. CDM testing is used to evaluate the ESD robustness of semiconductor devices, integrated circuits (ICs), and other electronic components. It is widely used in the semiconductor industry as a standard method for ESD testing. The CDM model assumes that the discharge current is essentially determined by the parasitic capacitances of the device and the discharge path, as well as the voltage difference between them. The discharge path can include the device's package, printed circuit board, and other components in the system.

The CDM test standard specifies the test waveform, the test conditions, and the pass/fail criteria for the device under test. The standard typically defines the minimum voltage level and number of discharges required for the device to be considered ESD safe. CDM testing is an important part of the ESD qualification process for electronic devices, as it can reveal potential weaknesses or failure modes that may not be detected by other ESD testing methods. [2]

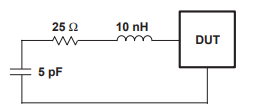


Figure 6. Equivalent Circuit of Discharge of the Charged-Device Model

In addition to these testing techniques, designers can use simulation tools to model the behavior of ESD protection circuits and optimize their design. Simulation tools such as SPICE can be used to model the behavior of ESD protection diodes, while more specialized tools such as EM field simulators can be used to model the propagation of electrical fields in analog layout circuits.

In addition to the above-mentioned approaches, designers can also use layout techniques to minimize the impact of ESD events on analog circuits. For example, signal paths can be separated and isolated from each other to prevent the propagation of ESD events through the circuit. This can be achieved through careful placement and routing of signal paths, as well as the use of shielding and guard rings to prevent noise and interference from surrounding circuits. [2]

**3.6.2 ESD protection in analog layout circuits: -**

There are two main types of ESD protection in analog layout circuits:

1. Device-level ESD protection - this involves adding structures within the device itself to protect against ESD. This includes structures such as diodes and transistors that are designed to withstand high voltage spikes.
2. Circuit-level ESD protection - this involves adding protection circuits to the overall design of the analog layout circuit. These circuits can take a variety of forms, including clamping circuits, active protection circuits, and capacitance-based protection circuits.

By incorporating ESD protection into analog layout circuits, potential damage to electronic components can be prevented or minimized, resulting in a more reliable and robust circuit.

One common approach to ESD protection in analog layout circuits is to add ESD protection diodes to signal paths. These diodes are designed to limit the dangerous voltages and conduct excess currents into regions of the circuit that are safe. The safe regions consist primarily of the supply-voltage connections. In the simplest case, the protection circuits consist of diodes that are oriented to be blocking in normal operation, and are situated between the connection to the component to be protected and the supply voltage lines (see Figure 7).

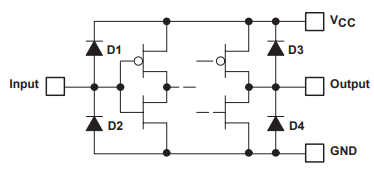


Figure 7. ESD-Protection Circuits Using Diodes

Another approach is to incorporate ESD protection into the design of the electronic devices themselves. For example, some transistors are designed to withstand higher voltage spikes than others, and can be used to protect sensitive components from ESD. In addition to these methods, there are also active ESD protection circuits that can be integrated into analog layout designs. These circuits are designed to detect and respond to ESD events in real-time, using techniques such as voltage clamping and current limiting to prevent damage. Figure 8 shows the complete input circuit, including the parasitic transistor. If a voltage () is applied to the input of this circuit that brings this transistor into a conducting state, an unwanted current flow from the input into the collector circuit of the input transistor. [2]

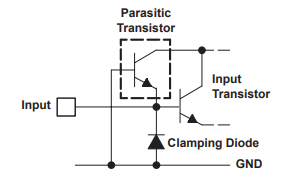


Figure 8. Input Circuit With Parasitic Transistor

**References**

1. Clein, Dan. CMOS IC layout: concepts, methodologies, and tools. Elsevier, 1999.‏
2. Haseloff, Eilhard. "Latch-up, ESD, and other Phenomena." Texas Instrument application report (2000).‏ (http://www.ti.com/lit/pdf/SLYA014)